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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,333	12/31/2003	Toshiaki Kiriata	0928.0068C	9607

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EXAMINER

SCHLIE, PAUL W

ART UNIT PAPER NUMBER

2186

DATE MAILED: 12/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/748,333	Applicant(s) KIRIHATA ET AL.	
	Examiner Paul W. Schlie	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-20 have been examined.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 2-3, 6-7, 10-14, 16 and 18 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure that is not enabling. Elements critical or essential to the practice of the invention, but not included in the claims are not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

As per claims 2-3, 6 and 16, although it is disclosed that the signal transmission delays which may otherwise result from more distantly placed memory arrays may be compensated for by operating such memories at higher voltages (which is considered obvious); however it is not disclosed and considered critical how correspondingly required regulated power at potentially arbitrarily required voltages may be cost effectively derived and/or distributed such that the technique disclosed may be practically implemented by one of ordinary skill in the art at the time of the claimed invention without undue experimentation, therefore not considered enabled.

As per claims 10-14, which seem related to the disclosed means by which memories which have different access times upon receiving a simultaneous access request may somehow simultaneously drive data onto a common signal line such that the two memory responses may be distinctly resolved, however not disclosed and

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considered a critical element not likely capable of being implemented by one of ordinary skill in the art at the time of the disclosed invention without undue experimentation; therefore not considered enabled.

As per claims 7 and 18, although it is considered obvious that various circuit implementations have different timing behaviors, and may be correspondingly utilized to optimize the performance of an memory system implementation; however it is not disclosed, considered critical, and not likely obvious to one of ordinary skill in the art at the time of the invention without undue experimentation, how a particular bit-line sensing circuit implementation which may correspondingly depend on a particular process (such as NMOS as disclosed) as seeming implied in the claims, may be practically utilized in a design implemented in a different process; therefore not considered enabled.

Corrective action is required, however new matter not supported by the original disclosure may not be added.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1-20, although attributes of a memory system are claimed, no clear elements with a distinct purpose beyond the obvious are claimed or strongly implied consistent with the disclosure (implying the claims may be too broadly constructed).

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Corrective action is required, however new matter not supported by the original disclosure may not be added.

Claim Rejections - 35 USC § 102/103

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-20 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Benini et al. ("From Architecture to Layout: Partitioned Memory Synthesis for Embedded Systems-on-Chip", June 2001 DAC).

As per claims 1, 8 and 15, Benini et al. teaches that a memory system may be automatically synthesized which may contain multiple memory arrays which may be composed of blocks of a larger logical memory, where each of which may correspondingly have a variety of differing properties either by original constraint, and/or as a result of the synthesis/selection/optimization process, including but not limited to: column/row organization, timing/performance, and power; based upon the temporal (i.e. frequency, performance and/or power goals), functional (i.e. volatile/non-volatile), and/or physical

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constraints (i.e. area, supply voltage, drive strength, impedance, placement, etc.); where their subcomponents, such as decode/control, and/or sense/driver elements, may correspondingly have differing properties in attempt to optimize the physical design in accordance with the aforementioned synthesis constraints and/or goals (see sections 3.1, 3.2, 3.3, 3.4; and although not cited as the basis of this rejection US Patent 6,324,678 also reviewing logical/physical system synthesis). Thereby it is considered inherent in that which is taught, and obvious to one of ordinary skill in the art at the time of the disclosed invention, that there are a variety of memory implementation design options which would enable a logical memory to be composed of a variety of physically distributed sub-memory elements such that the overall logical memory's partitioned implementation may have more optimal overall timing/performance/cost characteristics.

As per claims 2-6 and 16, being dependant on claim 1, 15, or correspondingly dependant claim inclusively; official notice is given that it is obvious to one of ordinary skill in the art that performance of semi-conductor logic is typically sensitive to supply voltage, and as such may be utilized to improve and/or attenuate the performance of a circuit at the corresponding expense and/or benefit of power consumption (although not typically utilized as the means to optimize/synchronize timing as implied in the disclosure and somewhat ambiguously in the claims, likely because it is considered not obvious to those ordinary skill in the art how to cost effectively derive and/or distribute a variety of voltages which may be utilized reliably in such a capacity upon which such a technique would depend, nor is enabled by the disclosure). Any potentially remaining

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claimed limitations not explicitly addressed are considered further considered obviously inherent in that taught, and/or not sufficient to patentably distinguish over prior art.

As per claims 9-14, being dependant on claim 8 or correspondingly dependant claim inclusively, official notice is given that it is obvious to one of ordinary skill in the art at the time of the disclosed invention that memory accesses and/or responses may be interleaved to improve data transfer bandwidth utilizing multiple memory banks (although not typically implemented as implied in the disclosure and ambiguous in the claims, likely because it is not considered obvious to one of ordinary skill in the art at the time of the claimed invention how such multiple banks of memory may, with different access times, reliably simultaneously drive a common physical signal line to achieve the stated results, nor enabled by the disclosure). Any potentially remaining claimed limitations not explicitly addressed are further considered obviously inherent in that taught, and/or not sufficient to patentably distinguish over prior art.

As per claims 7, 17-20, being dependant on claim 1, 15 or correspondingly dependant claim inclusively, official notice is given that it is obvious to one of ordinary skill in the art that different memory sense-amp and/or receiver/logic implementations have differing timing performance and may correspondingly be utilized as determined to be more optimal within an arbitrary design independently of other design choices (however it not considered obvious to one of ordinary skill in the art at the time of the disclosed invention how such choices may correspondingly depend on particular implementation process be arbitrarily utilized within a given implementation process as implied in the disclosure and ambiguous in the claims, nor enabled by the disclosure).

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Any potentially remaining claimed limitations not explicitly addressed are further considered obviously inherent in that taught, and/or not sufficient to patentably distinguish over prior art.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul W. Schlie whose telephone number is 571-272-6765. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



PIERRE BATAILLE
PRIMARY EXAMINER

12/21/05